## REMARKS

After entry of this amendment, claims 1-21, 23-30, and 32-33 remain pending. In the present Office Action, claim 21 was rejected under 35 U.S.C. § 112, second paragraph. Claims 1-21, 23-30, and 32-33 were rejected under the judicially-created doctrine of obviousness-type double patenting. Claims 1-21, 23-30, and 32-33 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yoshino et al., U.S. Patent No. 6,507,809 ("Yoshino"). Applicants respectfully traverse these rejections and request reconsideration.

Claims 1-20 and 24-29

Applicants respectfully submit that each of claims 1-20 and 24-29 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "wherein the plurality of nodes are configured to enter each phase concurrently and exit each phase concurrently, and wherein the plurality of nodes are configured to exit each phase in response to a command indicating that the phase is complete, and wherein each node of the plurality of nodes is configured not to cause the simulator program to evaluate a model of the different portion of the system under test during the first phase even if one or more commands are received by that node during the first phase, and wherein each node of the plurality of nodes is configured to cause the simulator program to evaluate the model during the second phase in response to receiving a command during the second phase, the command including one or more signal values for signals of the model".

The Office Action alleges that Yoshino anticipates the above features, citing Figs. 3B and 4-8 and Yoshino's text at col. 7, line 38-col. 9, line 2 and col. 9, line 9 to col. 11, line 8. With such a large section of Yoshino cited, it is difficult to discern what teachings of Yoshino are being relied on to allegedly anticipate each feature in the claims.

Nevertheless, Applicants note that Fig. 3B shows the simulators 302 and 303 executing at disjoint simulation times, each simulation time having a width of $\Delta t$. Yohsino teaches: "On the other hand, FIG. 3B shows how the performance simulation

system conducts performance simulation processes. The horizontal line with the arrow indicates the simulation time. First, the performance simulator 302 conducts a performance simulation process for a $\Delta t$ cycle that is equivalent to the segment 501, and upon end of the simulation process, the simulator 302 transmits shared resource occupation status data 505 to the performance simulator 303. Then, the performance simulator 303 simulates the performance of the partial unit 102 for which it is responsible for a $\Delta t$ cycle that is equivalent to the segment 502 while referring to the received shared resource data 505, and transmits shared resource data 506 to the performance simulator 302. Successively, the performance simulator 302 conducts a performance simulation process for another $\Delta t$ cycle that is equivalent to the segment 503, and thereafter repeats the afore-mentioned operations. (Yoshino, col. 7, lines 48-65). Thus, Fig. 3B and its description refer to one of the simulators being active and simulating for a time $\Delta t$ while the other simulator is stalled. This does not teach or suggest "the plurality of nodes are configured to enter each phase concurrently and exit each phase concurrently" as recited in claim 1.

Furthermore, each simulator executes to completion of the $\Delta t$ time period, and transmits shared resource data to the other simulator. Thus, there is no teaching that "the plurality of nodes are configured to exit each phase in response to a command indicating that the phase is complete".

Still further, the simulators transmit shared resource data to the other simulator, and the other simulator begins simulation and uses the resource data. When a simulator is not executing, it does not receive any commands. Accordingly, nothing with regard to Fig. 3B teaches or suggests "each node of the plurality of nodes is configured not to cause the simulator program to evaluate a model of the different portion of the system under test during the first phase even if one or more commands are received by that node during the first phase" as recited in claim 1.

With regard to Fig. 4, Yoshino teaches: "The performance simulation steps are proceeded along the vertical direction. The performance simulation system shown in

FIG. 1 *first* causes the performance simulator 302 to conduct a simulation process for a segment 601. It is supposed here that a shared resource occupation data 602 representing that the shared resource has been occupied is generated at a timing A. *Then*, the performance simulator 303 conducts a simulation process for a segment 603. In this case, the performance simulator 303 can consider the shared resource occupation data 602 at the timing A even during the simulation process for the segment 603. Further, it is supposed that a shared resource occupation data 604 is generated at a timing B during the same segment 603. In this case, the performance simulator 302 cannot consider the shared resource occupation data 604 at the timing B during its simulation process for the segment 601. That is, the simulator 302 can consider the shared resource occupation data 604 only at a timing C, which is the next synchronizing point." (Yoshino, col. 8, lines 13-32). Thus, Fig. 4 describes a similar simulation process to the process shown in Fig. 3B, merely depicted in a different way. For similar reasons to those given above, Fig. 4 and its description do not anticipate the above features of claim 1.

Fig. 8 is another timing diagram similar to Fig. 3B. With regard to Fig. 8, Yoshino teaches: "As shown in FIG. 8, the performance simulators 801 to 804 conduct performance simulation processes 1001 to 1004 for a $\Delta t$ cycle in parallel onto the processors for which they are responsible. When having finished the simulation processes, the performance simulators 801 to 804 cause the shared resource data transfer sections 306a to 306d to transmit shared resource data to the corresponding shared resource data transfer sections 307 to 310 of the performance simulator 805, and cause the synchronization control sections 703a to 703d to inform the synchronization control section 704 of the performance simulator 805 that the simulators 801 to 804 have finished the simulation processes for a $\Delta t$ cycle. After having been so informed by all the other performance simulators 801 to 804, the synchronization control section 704 causes the performance simulator 805 to start conducting a performance simulation process 1005 for a $\Delta t$ cycle onto the partial units for which the simulator 805 is responsible. Upon end of its simulation process, the performance simulator 805 transmits shared resource data to the shared resource data transfer sections 306a to 306d of the performance simulators 801 to 804 through the shared resource data transfer sections 307 to 310, and informs the

synchronization control sections 703a to 703d of the performance simulators 801 to 804 through the synchronization control section 704 that the simulator 805 has finished its simulation process." (Yoshino, col. 10, line 43-col. 11, line 2). Yohsino also teaches that the simulators 801-804 are independent of each other: "the processors 901 to 904 share no resource in common, and thus these processors operate independently of one another. Therefore, in the performance simulation system shown in FIG. 6, the performance simulators 801 to 804 have to communicate with the performance simulator 805 for shared resource management, while the performance simulators 801 to 804 do not have to communicate with one another for shared resource management. Hence, the performance simulators 801 to 804 can simulate the performances of the processors 901 to 904 independently as well as in parallel." (Yoshino, col. 10, lines 27-37).

Accordingly, the system depicted via Figs 5-8 is similar to the system depicted in Figs 3B and 4, in that any simulator that shares a resource with another simulator simulates in a different simulation time and provides the shared resource data to the other simulator. The system depicted in Figs. 5-8 merely shows that independent portions that do not communicate can simulate in parallel.

The simulators 801 to 804 simulate independently, and inform the simulator 805 when they have completed. Thus, each of the simulators 801 to 804 independently exits a simulation time $\Delta t$ even if other simulators are still simulating. This does not teach or suggest "the plurality of nodes are configured to enter each phase concurrently and exit each phase concurrently". Furthermore, the simulators 801 to 804 transmit commands indicating that they have completed simulation, but do not receive any command indicating that the $\Delta t$ simulation time has ended. These teachings do not teach or suggest "the plurality of nodes are configured to exit each phase in response to a command indicating that the phase is complete". Finally, simulators 801 to 804 execute at disjoint simulation times from simulator 804. Thus, the simulators 801 to 805 do not teach or suggest " the plurality of nodes are configured to enter each phase concurrently and exit each phase concurrently, and wherein the plurality of nodes are configured to exit each phase in response to a command indicating that the phase is complete, and wherein each

node of the plurality of nodes is configured not to cause the simulator program to evaluate a model of the different portion of the system under test during the first phase." At any given simulation time, at least one simulator is simulating and thus there is no phase that corresponds to the first phase.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-14 depend from claim 1, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 2-14 recites additional combinations of features not taught or suggested in the cited art.

Claim 15 recites a combination of features including: "process a first one or more commands received during a first phase of a timestep without causing a simulator program to evaluate a model, and cause the simulator program to evaluate the model during a second phase of the timestep in response to receiving a second command including one or more signal values for signals of the model, wherein the second command is received during the second phase of the timestep, and wherein the instructions, when executed, exit one of the first phase and second phase in response to receiving a third command indicating that the phase is complete". The same teachings of Yoshino highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 15. Applicants respectfully submit that Yoshino does not teach or suggest the above highlighted features of claim 15, either. Accordingly, claim 15 is patentable over the cited art. Claims 16-20, being dependent from claim 15, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 16-20 recites additional combinations of features not taught or suggested in the cited art.

Claim 24 recites a combination of features including: "receiving a first one or more commands in a node of a distributed simulation system during a first phase of a timestep; processing the first one or more commands without causing a simulator program to evaluate a model; receiving a second command during a second phase of the timestep; processing the second command including causing the simulator program to

evaluate the model if the second command includes one or more signal values for signals of the model; receiving a third command indicating that one of the first phase and the second phase is complete; and exiting the phase in response to the third command" The same teachings of Yoshino highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 24. Applicants respectfully submit that Yoshino does not teach or suggest the above highlighted features of claim 24, either. Accordingly, claim 24 is patentable over the cited art. Claims 25-29, being dependent from claim 24, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 25-29 recites additional combinations of features not taught or suggested in the cited art.

Claims 21, 23, 30, and 32

Applicants respectfully submit that each of claims 21, 23, 30, and 32 recite combinations of features not taught or suggested in the cited art. For example, claim 21 recites a combination of features including: "signal the end of either the first phase or the second phase *responsive to receiving a no-operation packet from each of the plurality of nodes* subsequent to transmitting a command other than a no-operation packet to at least one of the plurality of nodes".

The same teachings of Yoshino highlighted above with regard to claim 1 were alleged to teach the above highlighted features of claim 21. Applicants can find no teaching in the cited section, nor anywhere in Yoshino, of no-operation packets nor of using them in the manner recited above.

For at least the above stated reasons, Applicants submit that claim 21 is patentable over the cited art. Claim 23, being dependent from 21, is similarly patentable over the cited art for at least the above stated reasons as well. Claim 23 recites an additional combination of features not taught or suggested in the cited art.

Claim 30 recites a combination of features including: "signaling the end of the first phase is responsive to receiving a no-operation packet from each of the plurality of

nodes subsequent to transmitting a command other than a no-operation packet to at least one of the plurality of nodes". The same teachings of Yoshino highlighted above with regard to claim 23 are alleged to teach the above highlighted features of claim 30. Applicants respectfully submit that Yoshino does not teach or suggest the above highlighted features of claim 30, either. Accordingly, claim 30 is patentable over the cited art. Claim 32, being dependent from claim 30, is similarly patentable over the cited art for at least the above stated reasons. Claim 32 recites an additional combination of features not taught or suggested in the cited art.

Claim 33

Claim 33 recites a combination of features including: "the first node is configured to cause the simulator program to re-evaluate the model in response to receiving a second command including one or more signal values for signals of the model during the first timestep". The same teachings of Yoshino highlighted above with regard to claim 1 are alleged to teach the features of claim 33. Applicants can find no teaching in the cited section, nor anywhere in Yoshino, of re-evaluating a model in the same timestep in response to receiving additional signal values in a second command. For at least all of the above stated reasons, Applicants submit that claim 33 is patentable over the cited art.

Section 112 Rejection

The section 112 rejection of claim 21 asserted that the phrase "are configured to" after "instructions" creates ambiguity. Applicants have struck the phrase from claim 21. Additionally, the section 112 rejection suggests adding "when executed on the computer" after the second use of "instructions". Applicants have adopted the suggestion, and have amended claim 23 in a similar fashion. Applicants respectfully submit that the amendments address the section 112 rejection.

Double Patenting Rejection

The Office Action rejected the pending claims under the judicially-created doctrine of obviousness-type double patenting over claim 1 of three co-pending

applications: Serial Nos. 10/008,643 ("Application1"), 10/008,270 ("Application2"), and 10/008,255 ("Application3").

Applicants note that Application1 has issued as U.S. Patent No. 7,020,722. Claim 1 of the issued patent differs from claim 1 as cited in the rejection. For example, claim 1 of the issued patent recites features such as "wherein a simulation of the system under test comprises the plurality of nodes simulating the components, and wherein each node is configured to transmit a first command indicating that the node has completed simulation for a first timestep and thus that the node is capable of completing the first timestep; wherein a synchronized transition from the first timestep to a second timestep that follows the first timestep in the plurality of nodes is performed responsive to receiving the first command from each node of the plurality of nodes". Applicants respectfully submit that the pending claims of the present application are not properly rejected under obviousness type double patenting over claim 1 of the issued patent.

With respect to Application2, Applicants respectfully request that the rejection be held in abeyance until the claims are otherwise indicated as allowable. If Application2 remains pending, Applicants will consider the filing of a terminal disclaimer at that time.

Application3 is now abandoned. Accordingly, Applicants respectfully submit that the rejection with regard to Application3 is moot and should be withdrawn.

## CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-97900/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

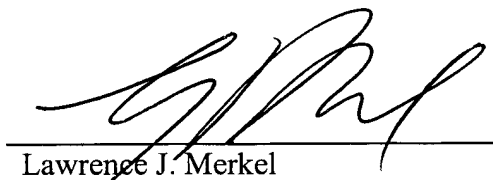
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Please debit the deposit account listed above in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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